REV.	ZONE	ECN#	REVISION	APPD	DATE
A			PRODUCTION RELEASE	D.H.	2/14/91

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	METRIC		Apple Computer, Inc.
DIMENSIONS ARE IN MILLIMETERS. DIMENSIONS IN BRACKETS [ ] ARE IN INCHES. TOLERANCES X.X ± 0.3 [.01] X.XX ± 0.13 [.005] X.XXX ± 0.03 [.001] ANGLEs ± 0.1 or as noted DO NOT SCALE DRAWING	DRAFT B.T. 2/13/91 / DESIGN CK 2/14/91 ENG APPD D.H. 2/14/91 / MFG APPD // QA APPD // / DESIGNER // RELEASE // / SCALE: NONE MATERIAL/FINISH NOTED AS APPLICABLE / SIZE A	NOTICE OF PROPRIETARY PROPERTY THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: (i) TO MAINTAIN THIS DOCUMENT IN CONFIDENCE (ii) NOT TO REPRODUCE OR COPY IT (iii) NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART TITLE: IC, APPLE // OPTION CHIP, 128-PIN PQFP DRAWING NUMBER 343S0111-A / SHT 1/22	

1.0 SCOPE: This specifies the parametric requirements for the Apple // Option Chip which provides the control circuitry and CPU host interface for the Apple // Emulation Card used by LC and possibly other future Macintosh computers.

It is implemented as a Gate-array using an LSI Logic Inc. LMA-9000 series 1.5 micron compacted-array in an 128-pin PQFP package.

The Apple // Option Chip provides support for all of the Apple //e functionality. This includes soft-switches, memory mapping, I/O card simulation, support for an external IWM and joystick port, and timing generation for an external 65C02. Apple //e video generation is not included because this function will be provided by software running on the Macintosh. The Apple // Option Chip provides an interface to the Macintosh so that the Apple //e functions can be monitored by software running on the Macintosh. When certain critical addresses are accessed by the 65C02, Apple // Option Chip captures the address and the data and temporarily halts the 65C02. A status flag to the Macintosh indicates that this "trap" has occured and the Macintosh can then read the address, data and other status information before allowing the 65C02 to continue. This process is used to capture all the video writes and most I/O accesses done by the 65C02 so that the Macintosh software can draw an appropriate Apple //e-like display on its screen.

The Apple // Option Chip supports 256K bytes of DRAM. This RAM is divided into a 128K byte space that represents the normal 128K Apple //e RAM, a 64K byte space that acts as an optional second 'Aux Bank' of Apple //e RAM, and a 64K byte space that acts like ROM and is partitioned into Apple ROM and I/O card ROM spaces. This ROM is normally writable from the Macintosh and not from the 65C02.

Since there is no ROM on card, Apple // Option Chip includes the capability of running from an external ROM or EPROM for burn-in testing. This external ROM is wired to the pins that would normally connect to the Macintosh address and data signals. When the external ROM is enabled, the trapping function described above is disabled and the 'ROM' areas of RAM are write-enabled so they can be tested by the 65C02.

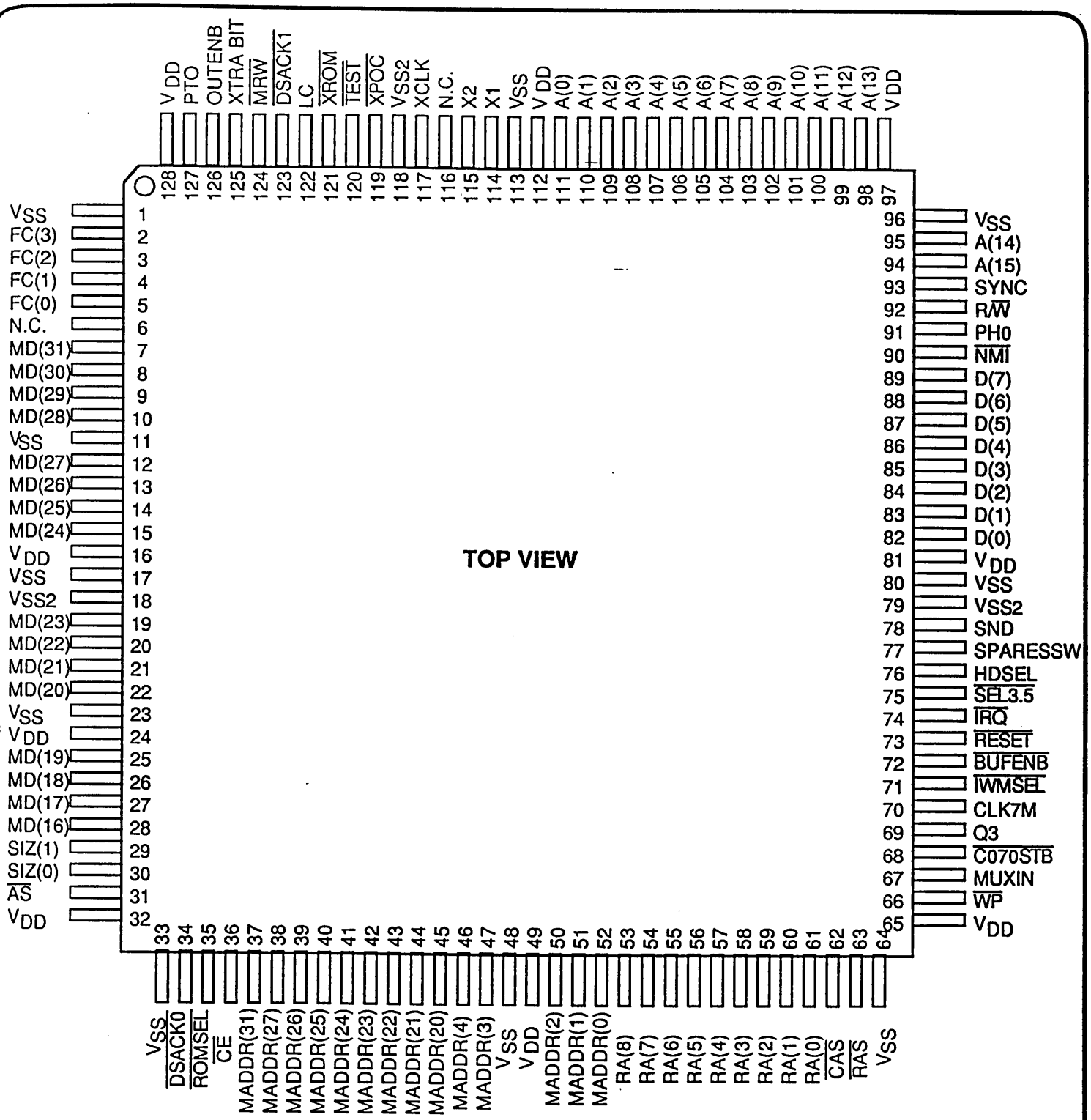


FIGURE 1. PIN CONFIGURATION

Apple Computer, Inc.

SIZE	DRAWING NUMBER
A	343S0111-A
SCALE: NONE	SHT 3 OF 22

TABLE 1. PIN DESCRIPTION

68020 CPU Bus Interface			
SIGNAL	**TYPE**	**DESCRIPTION**	**PIN #'S**
$\overline{AS}$	input	CPU address strobe	31
$\overline{MRW}$	input	CPU data bus direction	124
MADDR(31)	input	CPU upper address bits	37
MADDR(27)	input	CPU upper address bits	38
MADDR(26)	input	CPU upper address bits	39
MADDR(25)	input	CPU upper address bits	40
MADDR(24)	input	CPU upper address bits	41
MADDR(23)	input	CPU upper address bits	42
MADDR(22)	input	CPU upper address bits	43
MADDR(21)	input	CPU upper address bits	44
MADDR(20)	input	CPU upper address bits	45
MADDR(4)	input	CPU lower address bits	46
MADDR(3)	input	CPU lower address bits	47
MADDR(2)	input	CPU lower address bits	50
MADDR(1)	input	CPU lower address bits	51
MADDR(0)	input	CPU lower address bits	52
MD(31)	input/output - 8ma	CPU Data bus upper word	7
MD(30)	input/output - 8ma	CPU Data bus upper word	8
MD(29)	input/output - 8ma	CPU Data bus upper word	9
MD(28)	input/output - 8ma	CPU Data bus upper word	10
MD(27)	input/output - 8ma	CPU Data bus upper word	12
MD(26)	input/output - 8ma	CPU Data bus upper word	13
MD(25)	input/output - 8ma	CPU Data bus upper word	14
MD(24)	input/output - 8ma	CPU Data bus upper word	15
MD(23)	input/output - 8ma	CPU Data bus upper word	19
MD(22)	input/output - 8ma	CPU Data bus upper word	20
MD(21)	input/output - 8ma	CPU Data bus upper word	21
MD(20)	input/output - 8ma	CPU Data bus upper word	22
MD(19)	input/output - 8ma	CPU Data bus upper word	25
MD(18)	input/output - 8ma	CPU Data bus upper word	26
MD(17)	input/output - 8ma	CPU Data bus upper word	27
MD(16)	input/output - 8ma	CPU Data bus upper word	28
FC(3)	input	CPU function code	2
FC(2)	input	CPU function code	3
FC(1)	input	CPU function code	4
FC(0)	input	CPU function code	5
$\overline{DSACK0}$	output(bidirect) - 4ma	CPU Data acknowledge: 8-bit	34
$\overline{DSACK1}$	output(bidirect) - 4ma	CPU Data acknowledge: 16-bit	123
SIZ(1)	input	CPU transfer size code	29
SIZ(0)	input	CPU transfer size code	30
$\overline{CE}$	input	Chip enable $\overline{ROM}$ enable select	36
LC	input	Address decode mode control	122

TABLE 1. PIN DESCRIPTION (CONT)

DRAM Interface			
SIGNAL	**TYPE**	**DESCRIPTION**	**PIN #'S**
RA(8)	output - 6ma	DRAM multiplexed address bus	53
RA(7)	output - 6ma	DRAM multiplexed address bus	54
RA(6)	output - 6ma	DRAM multiplexed address bus	55
RA(5)	output - 6ma	DRAM multiplexed address bus	56
RA(4)	output - 6ma	DRAM multiplexed address bus	57
RA(3)	output - 6ma	DRAM multiplexed address bus	58
RA(2)	output - 6ma	DRAM multiplexed address bus	59
RA(1)	output - 6ma	DRAM multiplexed address bus	60
RA(0)	output - 6ma	DRAM multiplexed address bus	61
$\overline{RAS}$	output - 6ma	DRAM row address strobe	63
$\overline{CAS}$	output - 6ma	DRAM column address strobe	62
$\overline{WP}$	output - 6ma	DRAM write enable	66
65C02 Interface			
SIGNAL	**TYPE**	**DESCRIPTION**	**PIN #'S**
A(15)	input	65C02 address bus	94
A(14)	input	65C02 address bus	95
A(13)	input	65C02 address bus	98
A(12)	input	65C02 address bus	99
A(11)	input	65C02 address bus	100
A(10)	input	65C02 address bus	101
A(9)	input	65C02 address bus	102
A(8)	input	65C02 address bus	103
A(7)	input	65C02 address bus	104
A(6)	input	65C02 address bus	105
A(5)	input	65C02 address bus	106
A(4)	input	65C02 address bus	107
A(3)	input	65C02 address bus	108
A(2)	input	65C02 address bus	109
A(1)	input	65C02 address bus	110
A(0)	input	65C02 address bus	111
D(7)	input/output - 6ma	65C02 data bus	89
D(6)	input/output - 6ma	65C02 data bus	88
D(5)	input/output - 6ma	65C02 data bus	87
D(4)	input/output - 6ma	65C02 data bus	86
D(3)	input/output - 6ma	65C02 data bus	85
D(2)	input/output - 6ma	65C02 data bus	84
D(1)	input/output - 6ma	65C02 data bus	83
D(0)	input/output - 6ma	65C02 data bus	82
R/$\overline{W}$	input	65C02 data bus direction	92
SYNC	input	65C02 clock	93
PH0	output - 4 ma	65C02 clock	91
$\overline{RESET}$	output - 4 ma	65C02 Reset	73
$\overline{IRQ}$	output - 4 ma	65C02 interrupt	74
$\overline{NMI}$	output - 4 ma	65C02 non-maskable interrupt	90
$\overline{BUFENB}$	output - 4 ma	65C02 bus buffer enable	72

TABLE 1. PIN DESCRIPTION (CONT)

I/O and test functions			
SIGNAL	**TYPE**	**DESCRIPTION**	**PIN #'S**
CLK7M	output - 4ma	7 MHz clock to IWM	70
Q3	output - 4ma	2 MHz clock to IWM	69
$\overline{\text{IWMSEL}}$	output - 4ma	IWM select signal	71
$\overline{\text{SEL3.5}}$	output - 8ma	3.5" drive select	75
$\overline{\text{HDSEL}}$	output - 8ma	3.5" drive head select	76
$\overline{\text{C070STB}}$	output - 4ma	Game port timer trigger	68
XTRA BIT	output - 8ma	Output port bit - Mac side	125
SPARESSW	output - 8ma	Output port bit - 65C02 side	77
MUXIN	input	Joystick mux output	67
$\overline{\text{SND}}$	output - 4ma	Apple //e spkr toggle output	78
$\overline{\text{ROMSEL}}$	output - 4ma	Chip enable for ext. config. ROM	35
PTO	output - 2ma	Input Threshold test output	127
X1	output	Xtal osc input	114
X2	input	Xtal osc output	115
XCLK	input	Main clock - 14MHz	117
$\overline{\text{OUTENB}}$	input	Disables all outputs when low	126
$\overline{\text{XPOC}}$	schmitt input	Power-on-clear	119
$\overline{\text{TEST}}$	input	enables DSACK test mode	120
$\overline{\text{XROM}}$	input	activates external ROM circuitry	121

Power			
SIGNAL	**TYPE**	**DESCRIPTION**	**PIN#'S**
V_{SS}	power	Pad-ring V_{SS} - Gnd	1, 11, 17, 23, 33, 48, 64, 80, 96, 113
V_{SS2}	power	Core V_{SS} - Gnd	18, 79, 118
V_{DD}	power	+5V	16, 24, 32, 49, 65, 81, 97, 112, 128

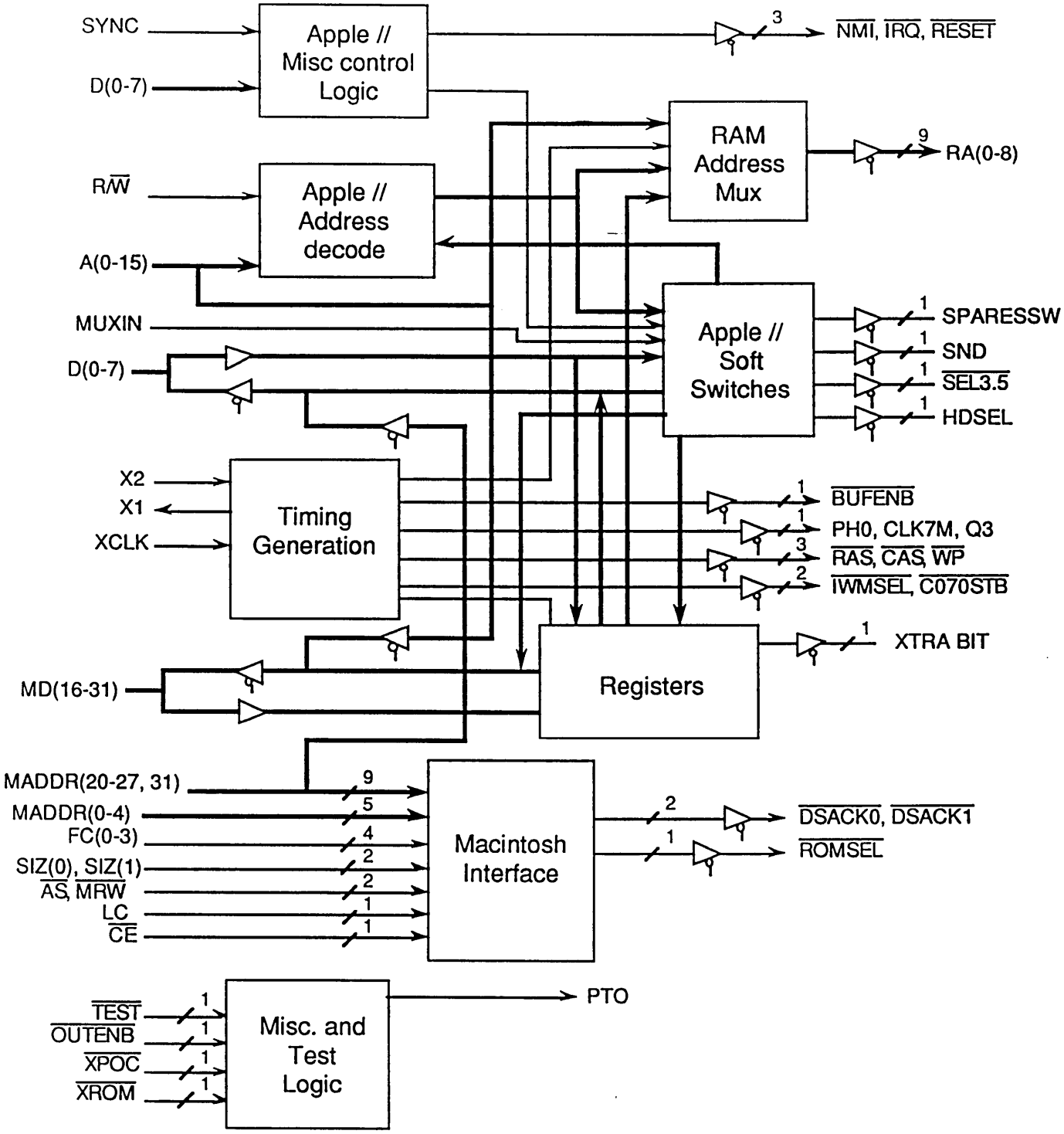


FIGURE 2. BLOCK DIAGRAM

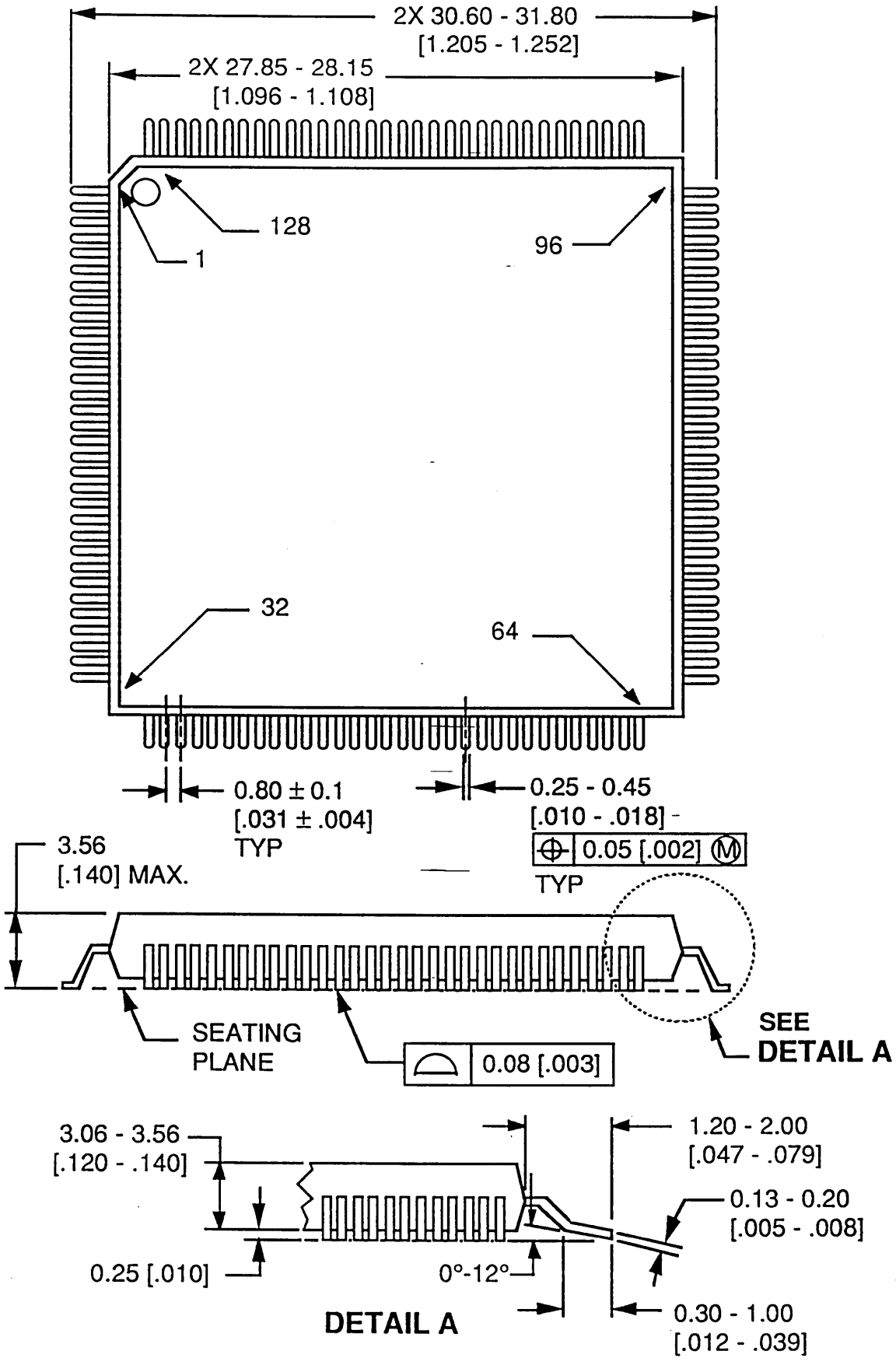


FIGURE 3. DIMENSIONS

Apple Computer, Inc.

SIZE	DRAWING NUMBER
A	343S0111-A
SCALE: NONE	SHT 8 OF 22

2.0 APPLICABLE DOCUMENTS (latest revision):

MIL-STD-202 Test methods for electronic and electrical component parts.

MIL-STD-883 Test methods and procedures for microelectronics.

3.0 REQUIREMENTS:

3.1 PHYSICAL:

3.1.1 **PACKAGE:** Void free plastic 128-pin PQFP package. Dimensions per Figure 3.

3.1.2 **MARKINGS:** Manufacturer's name or logo and manufacturing date code, Apple part number, current revision level, mask and copyright symbols, year and Apple name or logo.

EXAMPLE: 343S0111-A

Ⓜ Ⓒ 1990 Apple

3.1.3 **SOLDERABILITY:** Leads solderability must meet MIL-STD-202, Method 208.

3.2 ELECTRICAL:

3.2.1 **ELECTROSTATIC DISCHARGE SENSITIVITY:** The minimum electrostatic discharge voltage per pin is ±2000 volts as specified in MIL-STD-883, method 3015.3 (i.e., C = 100 pF, R = 1.5KΩ).

3.2.2 **LATCH-UP TEST:** The minimum latch-up current for all pins except ground is 50mA in both positive and negative directions. This applies to full temperature and power supply ranges.

3.2.3 **PIN CONFIGURATION:** Per Figure 1.

3.2.4 **PIN DESCRIPTION:** Per Table 1.

3.2.5 **BLOCK DIAGRAM:** Per Figure 2.

3.2.6 **ABSOLUTE MAXIMUM RATINGS:** Per Table 2.

3.2.7 **RECOMMENDED OPERATING CONDITIONS:** Per Table 3.

3.2.8 **STATIC PARAMETERS:** Per Table 4.

3.2.9 **DYNAMIC PARAMETERS:** Per Table 5, and Figure 4.

3.3 ENVIRONMENTAL:

3.3.1 **RESISTANCE TO SOLDERING HEAT:** 260°C for 10 sec in molten solder after 218°C for 30 sec in vapor phase, 60/40 solder and 260°C for 10 sec in molten solder after 240°C for 30 sec in I.R., 60/40 solder. Rate of temperature rise is 3°C/sec to within 100°C of the final temperature.

3.3.2 **CLEANING:** Parts must be washable in standard flux removal solvent and must not trap any cleaning liquids.

4.0 **QUALITY ASSURANCE PROVISIONS:** Parts shall be inspected to assure compliance to the requirements of this specification.

5.0 **PACKAGING:** Parts shall be packaged according to requirements specified in purchase order for safe delivery at Apple or Apple designated contractor. (Parts requiring Tape & Reel shall meet the proper Tape & Reel specification per the purchase order.)

TABLE 2. ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{DD}	-0.3 to 7.0	V
Input Voltage	V_{IN}	-0.3 to (V_{DD} + 0.3)	V
Operating Temp	T_A	0 to 70	°C
Storage Temp	T_S	-40 to 125	°C

TABLE 3. RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{DD}	5.0 ± 5%	V
Input Voltage	V_{IN}	0 to 5	V
Operating Temp	T_A	0 to 70	°C

TABLE 4. STATIC PARAMETERS

(V_{DD} = 5.0V, V_{SS} = 0V, T_A = 0°C to +70°C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
Input high voltage (Non-Schmitt inputs)	V_{IH}	V_{DD} = 4.75 V	2.0		V
Input low voltage (Non-Schmitt inputs)	V_{IL}	V_{DD} = 5.25 V		0.8	V
Input hysterisis (Schmitt inputs - $\overline{\text{DSACK0}}$, $\overline{\text{DSACK1}}$, and $\overline{\text{XPOC}}$)	V_{HST}	V_{DD} = 4.75 V	1.0	1.5	V
Input buffer leakage	I_{IN}	V_{IN} = 0 to V_{DD}, V_{DD} = 5.25 V	-10	+10	µA
Output buffer leakage (when tristated)	I_{OZ}	V_{OUT} = 0 to V_{DD}, V_{DD} = 5.25 V	-10	+10	µA

TABLE 4. STATIC PARAMETERS (CONT)

(V_{DD} = 5.0V, V_{SS} = 0V, T_A = 0°C to +70°C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
Output voltage (16 mA outputs)	V_{OL}	I_{OL} = -16 mA V_{DD} = 4.75 V		0.4	V
Output voltage (8 mA outputs)	V_{OL}	I_{OL} = -8 mA V_{DD} = 4.75 V		0.4	V
Output voltage (4 mA outputs)	V_{OL}	I_{OL} = -4 mA V_{DD} = 4.75 V		0.4	V
Output voltage (2 mA outputs)	V_{OL}	I_{OL} = -2 mA V_{DD} = 4.75 V		0.4	V
Output voltage (16 mA outputs)	V_{OH}	I_{OL} = 16 mA	2.4		V
		I_{OL} = 8 mA V_{DD} = 4.75 V	3.5		V
Output voltage (8 mA outputs)	V_{OH}	I_{OL} = 8 mA	2.4		V
		I_{OL} = 4 mA V_{DD} = 4.75 V	3.5		V
Output voltage (4 mA outputs)	V_{OH}	I_{OL} = 4 mA	2.4		V
		I_{OL} = 12 mA V_{DD} = 4.75 V	3.5		V
Output voltage (2 mA outputs)	V_{OH}	I_{OL} = 2 mA	2.4		V
		I_{OL} = 1 mA V_{DD} = 4.75 V	3.5		V
Input Capacitance	C_{IN}	V_{IN}=0, T_A=25°C, f=1 MHz		10	pF
Output Capacitance	C_{TS}	V_{OUT}=0, T_A=25°C, f=1 MHz		10	pF
Supply current (No load)	I_{CC}	Clock = 14MHz		25	mA
Standby Current	I_{SBY}	Outputs unloaded. Clock = 0 MHz		10	µA

TABLE 5. DYNAMIC PARAMETERS

(V_{DD} = 5.0V, V_{SS} = 0V, T_A = 0°C to +70°C, unless otherwise noted)

A.C. PARAMETERS

NO.	INPUT	TO OUTPUT	MIN	TYP	MAX	UNIT	LOAD (pF)	NOTES
1	Clock period	- n/a -	65	70	∞	ns		
1a	Clock high period	- n/a -	25	35	∞	ns		
1b	Clock low period	- n/a -	25	35	∞	ns		
1c	Clock Rise/Fall time	- n/a -		5	10	ns		
2	Clock	PH0			20	ns	35	1.
3	Clock	$\overline{RAS}$, $\overline{CAS}$, $\overline{WP}$			25	ns	50	2.
4	Clock	RA(0-8)			35	ns	50	2.
5	Clock	Gen. Clk'd outputs			40	ns	50	3., 4.
6	Clock	D(0-7) (turn on or chg.)			30	ns	50	
7	Clock	D(0-7) Hi-Z			40	ns	50	
8	A(0-15)	RA(0-8) when $\overline{RAS}$ active			30	ns	50	
9	A(0-15)	RA(0-8) when $\overline{CAS}$ active			40	ns	50	
10	A(0-15)	MD(16-31)			25	ns	100	6.
11	A(0-15)	A2 Decoded outputs			30	ns	50	
12	MD(16-31)	D(0-7)			25	ns	50	6.
13	$\overline{AS}$(high)	MD(16-31) Hi-Z			15	ns	100	
14	Outenb	All disablable outputs			30	ns		6.

A.C. OPERATING CONDITIONS - INPUT SETUP TIME REQUIREMENTS

NO.	INPUT SETUP	RELATIVE TO INPUT	MIN	TYP	MAX	UNIT	LOAD (pF)	NOTES
15	Mac Addrs. Inputs	$\overline{AS}$ falling edge			0	ns		
16	65C02 addrs inputs	Clock rising edge			35	ns		5.
17	D(0-7)	Clock rising edge			13	ns		
18	MD(16-31)	Clock rising edge			10	ns		

A.C. OPERATING CONDITIONS - INPUT HOLD TIME REQUIREMENTS

NO.	INPUT HOLD	RELATIVE TO INPUT	MIN	TYP	MAX	UNIT	LOAD (pF)	NOTES
19	Mac Addrs. Inputs	$\overline{AS}$ rising edge	10			ns		
20	65C02 addrs inputs	Clock rising edge	5			ns		5.
21	D(0-7), MD(16-31)	Clock rising edge	5			ns		

NOTES:

1. General clocked outputs are: SND, $\overline{IRQ}$, $\overline{NMI}$, $\overline{RESET}$, $\overline{BUFENB}$, $\overline{WP}$, $\overline{DSACK0}$, $\overline{DSACK1}$, CLK7M, Q3, $\overline{C070STB}$, $\overline{SEL3.5}$, HDSEL, XTRA BIT, SPARESSW,
2. A2 decoded outputs are: $\overline{IWMSEL}$, $\overline{C070STB}$,
3. Mac addrs inputs are: SIZ(0), SIZ(1), FC(0-3), MADDR(0-4), MADDR(20-27), MADDR(31)
4. 65C02 Addrs inputs are: A(0-15), R/$\overline{W}$, SYNC
5. Setup times for 65C02 addrs inputs are setups to the relevant clock edge.
6. Used for factory testing only.

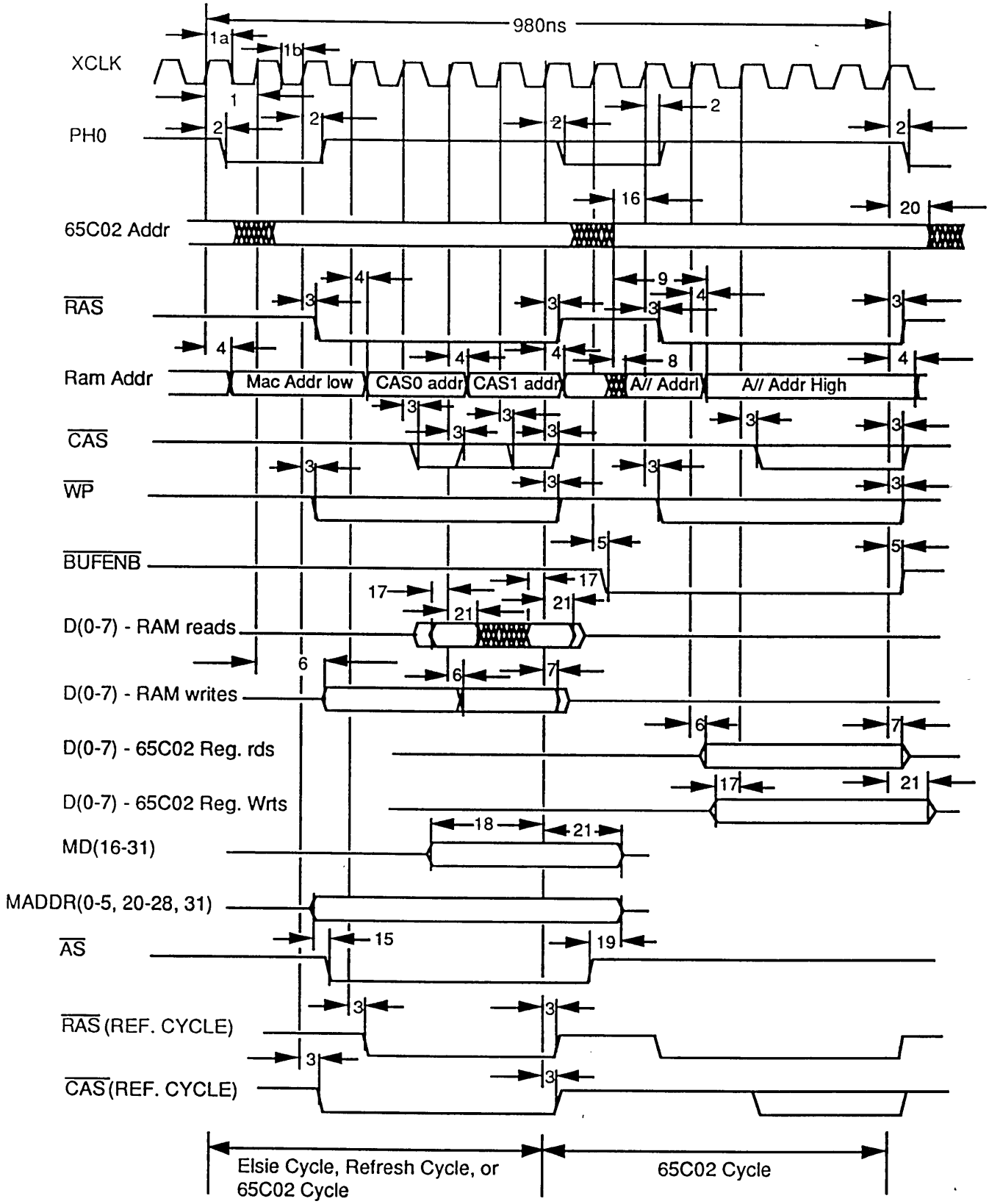


FIGURE 4. TIMING DIAGRAM

Apple Computer, Inc.

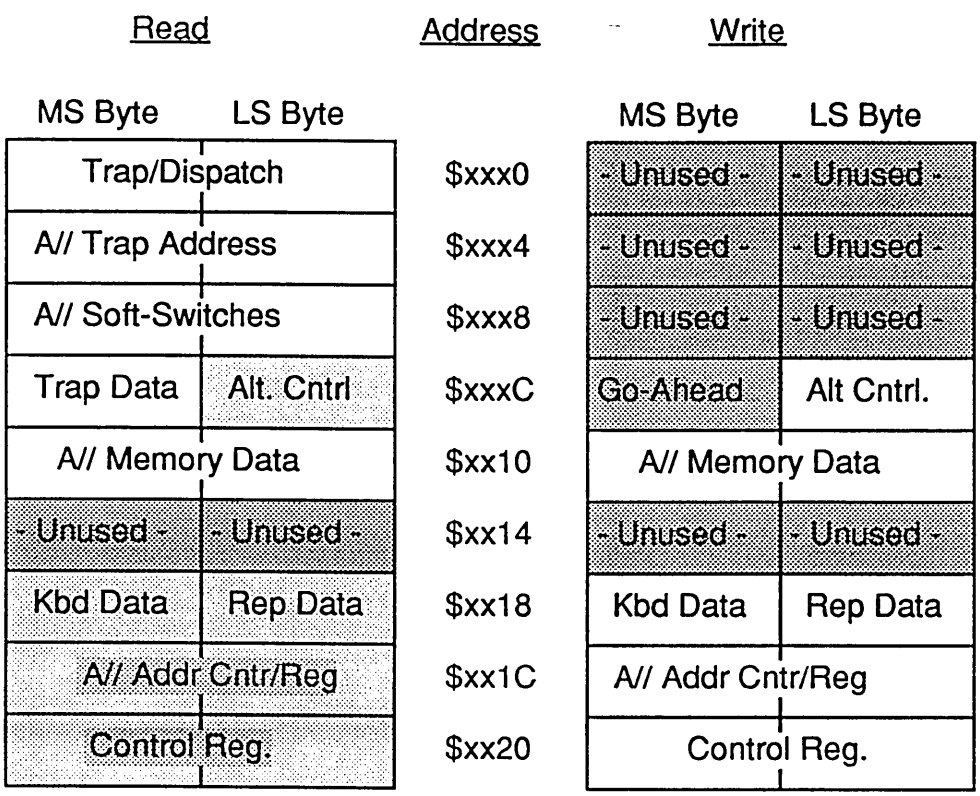
SIZE	DRAWING NUMBER
A	343S0111-A
SCALE: NONE	SHT 13 OF 22

6.0 SUPPLEMENTARY INFORMATION: The following is not to be used for the acceptance or rejection of the part herein.

6.1 OPERATIONAL DESCRIPTION:

6.1.1 MACINTOSH VIEW OF APPLE // EMULATION CARD:

Apple // Emulation Card looks as much as possible like an Apple //e to the 65C02 microprocessor and looks like a set of I/O registers to the Macintosh.



Indicates currently unused.

Indicates register supported for test purposes

FIGURE 5. APPLE // OPTION CHIP REGISTER MAP

NOTE:

7. The addresses shown above are offsets from the LC or other Macintosh I/O slot base address. When the 65C02 accesses certain key I/O locations or writes to the Apple //e display areas, it is "Trapped" (or halted temporarily) and the address accessed and data read or written is latched so that the information is available to the Macintosh. After the Macintosh has gathered the data, it accesses the "GoAhead" location or writes to the Read Data Replacement register to allow the 65C02 to continue. The Apple // Emulation Card also provides a "Hint" mode which can be enabled in place of traps for 65C02 video writes. Traps are disabled when the Disk Motor-On switch is true, so that code accessing the IWM chip will not be disturbed. Hint mode captures the address and data written, but does not halt the 65C02. The current hint is cleared when the Macintosh reads the Trap Address register further below.

6.1.2 THE TRAP/DISPATCH/STATUS REGISTER:

Read only Addr: Base + xxxx0 Size: 16-bits

This register provides information describing the type of trap that has occured. It reads zero when 65C02 is not trapped. When non-zero, the value in the register may be used directly to index into a table of long addresses to vector qūickly to the appropriate trap handler. The Trap/dispatch codes are provided in the lower byte only.

TABLE 6. TRAP/DISPATCH REGISTER CODES

TRAP TYPE	DISPATCH CODE	TRAP TYPE	DISPATCH CODE
No Trap	d^1d^0 000 000	Soft-Sw Write	d^1d^0 100 000
** unassigned	d^1d^0 000 001	Soft-Sw Read	d^1d^0 100 001
Txt Wr. main Pg1 Trp	d^1d^0 000 010	Txt Wr. main PG2 Trp	d^1d^0 100 010
Txt Wr. main Pg1 Hint	d^1d^0 000 011	Txt Wr. main PG2 Hint	d^1d^0 100 011
HiRes Wr. main Pg1 Trap	d^1d^0 000 100	HiRes Wr. main Pg2 Trap	d^1d^0 100 100
HiRes Wr. main Pg1 Hint	d^1d^0 000 101	HiRes Wr. main Pg2 Hint	d^1d^0 100 101
** unassigned	d^1d^0 000 110	** unassigned	d^1d^0 100 110
** unassigned	d^1d^0 000 111	** unassigned	d^1d^0 100 111
I/O Slot Hdw. write	d^1d^0 001 000	$C0E8 Write	d^1d^0 101 000
I/O slot Hdw. read	d^1d^0 001 001	$C0E8 Read	d^1d^0 101 001
Text Wr. Aux Pg1 Trap	d^1d^0 001 010	Txt Wr. aux Pg2 Trp	d^1d^0 101 010
Text Wr. Aux Pg1 Hint	d^1d^0 001 011	Txt Wr. aux Pg2 Hint	d^1d^0 101 011
HiRes Wr. Aux Pg1 Trap	d^1d^0 001 100	HiRes Wr. aux Pg2 Trap	d^1d^0 101 100
HiRes Wr. Aux Pg1 Hint	d^1d^0 001 101	HiRes Wr. aux Pg2 Hint	d^1d^0 101 101
** unassigned	d^1d^0 001 110	** unassigned	d^1d^0 101 110
** unassigned	d^1d^0 001 111	** unassigned	d^1d^0 101 111
S0 $C8-Space write	d^1d^0 010 000	** unassigned	d^1d^0 110 000
S0 $C8-Space Read	d^1d^0 010 001	** unassigned	d^1d^0 110 001
S2 $C8-Space write	d^1d^0 010 010	** unassigned	d^1d^0 110 010
S2 $C8-Space Read	d^1d^0 010 011	** unassigned	d^1d^0 110 011
S4 $C8-Space write	d^1d^0 010 100	** unassigned	d^1d^0 110 100
S4 $C8-Space Read	d^1d^0 010 101	** unassigned	d^1d^0 110 101
S6 $C8-Space write	d^1d^0 010 110	** unassigned	d^1d^0 110 110
S6 $C8-Space Read	d^1d^0 010 111	** unassigned	d^1d^0 110 111
S1 $C8-Space write	d^1d^0 011 000	$C0E9 Write	d^1d^0 111 000
S1 $C8-Space Read	d^1d^0 011 001	$C0E9 Read	d^1d^0 111 001
S3 $C8-Space write	d^1d^0 011 010	** unassigned	d^1d^0 111 010
S3 $C8-Space Read	d^1d^0 011 011	** unassigned	d^1d^0 111 011
S5 $C8-Space write	d^1d^0 011 100	** unassigned	d^1d^0 111 100
S5 $C8-Space Read	d^1d^0 011 101	** unassigned	d^1d^0 111 101
S7 $C8-Space write	d^1d^0 011 110	** unassigned	d^1d^0 111 110
S7 $C8-Space Read	d^1d^0 011 111	** unassigned	d^1d^0 111 111

NOTE:

8. d^1 and d^0 are two bits in the Alt Control Register that can be used by the programmer to select one of four dispatch tables.

TABLE 7. TRAPPED APPLE //e ACCESSES

Display Areas:

ADDRESS	R/W	DESCRIPTION	COMMENTS
$400-7FF	Write	Text/LoRes pg1 stores	Maskable for main/aux
$800-BFF	Write	Text/LoRes pg2 stores	Maskable for main/aux
$2000-3FFF	Write	HiRes/Dbl-Hires pg1 stores	Maskable for main/aux
$4000-5FFF	Write	HiRes/Dbl-Hires pg2 stores	Maskable for main/aux

Internal Soft-Switch and I/O Areas:

ADDRESS	R/W	DESCRIPTION	COMMENTS
$C000,1	Write	80Store Soft-sw	Non-maskable - Affects display
$C00C-D	Write	80Col soft-sw	Non-maskable - Affects display
$C00E-F	Write	AltCharSet soft-sw	Non-maskable - Affects display
$C040-F	R/W	Spare Soft-switch area	Non-maskable
$C050-57	R/W	Display soft-sw's	Non-maskable - Affects display
$C058-5F	R/W	Announciators	Non-maskable - AN3 Affects display
$C060-67	R/W	Joy-Stick Pdls & Swtchs.	Maskable
$C070-7F	R/W	JoyStick Trig and spares	Non-maskable

I/O Slot accesses:

ADDRESS	R/W	DESCRIPTION	COMMENTS
$C090-9F	R/W	Slot 1 Hardware accesses	Non-maskable - For card simulation
$C0A0-AF	R/W	Slot 2 Hardware accesses	Non-maskable - For card simulation
$C0B0-BF	R/W	Slot 3 Hardware accesses	Non-maskable - For card simulation
$C0C0-CF	R/W	Slot 4 Hardware accesses	Non-maskable - For card simulation
$C0D0-DF	R/W	Slot 5 Hardware accesses	Non-maskable - For card simulation
$C0E8-E9	R/W	Slot 6 Motor on/off switch	Non-maskable - 5.25" Motor on/off
$C0F0-FF	R/W	Slot 7 Hardware accesses	Non-maskable - For card simulation
$C800-CFFE	R/W	Shared 2K $C8-Space	Maskable - For card simulation
$CFFF	R/W	Shared $C8-Space switch.	Non-maskable - For card simulation

NOTES:

9. The "Screen-Hole" areas in the above address ranges do not trap. These are the $xx78-7F and $xxF8-FF address ranges in the display areas.
10. Display writes do not trap when the Slot 6 motor switch is 'on'.
11. Display writes may optionally cause 'hints' instead of traps if Hint mode is enabled in the Apple // Emulation Card Control register.
12. $CFFF accesses produce $C8-Space dispatch codes in the trap dispatch register. The dispatch code will indicate which slot ROM space was most recently accessed before the $C8-Space access occured.

6.1.3 THE TRAP REGISTER:

Read only Addr: Base + xxxx4 Size: 16-bits

Bits 0-7: The L.S. byte of the Apple //e address trapped.
Bits 8-15: The M.S. byte of the Apple //e address trapped.

Reading a byte from addr B+xxx4 will provide the high byte of the Apple // trap address.

Reading a byte from addr B+xxx5 will provide the low byte of the Apple // trap address.

NOTES:

13. The data in this register will only be valid and stable while the Apple // is trapped or stopped, or when the hint flag in the Apple // Emulation Card Control Register is set.
14. This register only provides the 16-bit 65C02 address that was present when the trap occured. It does not indicate whether the 65C02 was accessing the main 64K or aux 64K RAM bank, however the Main/Aux information is implicit in the Trap/Dispatch code generated.

6.1.4 THE SOFT-SWITCH REGISTER

Read only Addr: Base + xxxx8 Size: 16-bits

This register allows the LC software to read the state of the Apple //e soft-switches.

BIT	DESCRIPTION	BIT	DESCRIPTION
15	AltCharSet-Sw	7	KbdFlg
14	Text Sw	6	An1 Sw
13	Hi-Res Sw	5	An0 Sw
12	AN3 Sw	4	SlotC3ROM Sw
11	80COl Sw	3	IntCxROM Sw
10	Mixed Sw	2	AltZP Sw
9	Page2 Sw	1	RAMWrt Sw
8	80Store Sw	0	RAMRd Sw

Reading a byte from addr B+xxx8 will provide the high byte of the Apple // soft-switch status.

Reading a byte from addr B+xxx9 will provide the low byte of the Apple // soft-switch status.

6.1.5 THE TRAP DATA REGISTER

Read only Addr: Base + xxxxC Size: 8-bits

Bits 0-7: The byte of the Apple //e data being read or written when the Apple // trapped.

NOTE:

15. The data in this register is only valid when the Apple // is trapped or stopped or when the Hint Flag in the Apple // Emulation Card Control Register is set.

6.1.6 THE ALT. CONTROL REGISTER

Read/Write Addr: Base + xxxxD Size: 8-bits

This register allows the LC to control various aspects of the Apple // Emulation Card card operation. There is an additional 16-bit control register at loc $B+xxx20.

Reads are supported to facilitate testing and simply return the last value written.

BIT DESCRIPTION

7 AKD - Any-Key-Down signal to Apple II side.
6 VBL signal to 65C02 programs
5 Enable alternate 65C02 16K byte DarkSide ROM bank
4 Enable ROM writes from 65C02.
3 Select Hi bank 128K RAM bank for read/write access
2 Enable alternate 64K Apple II Aux Bank.
1 D1
0 D0

NOTE:
16. Bits 1 and 0 are the d^1d^0 bits used in Table 6.

6.1.7 THE MEMORY DATA REGISTER

Read/Write Addr: Base + xxx10 Size: 16-bits

This register or used to read or write the Apple // RAM. Bits 0-7 read/write the Aux 64K bank of RAM and bits 8-15 read/write the Main 64K bank. Each time this register is accessed, the pointer address stored in the RAM Address latch/counter register is incremented, so that contiguous blocks of data can be moved to or from the Apple // RAM with a series of sequential read or writes to the Memory data register.

6.1.8 THE KEYBOARD DATA REGISTER

Read/Write Addr: Base + xxx18 Size: 8-bits

Bit 7: - Unused -
Bits 0-6: 7 bits of simulated Apple //e ASCII keyboard data.

Writes to this register simulate keystrokes on the Apple // keyboard. When a key on the LC keyboard is pressed, the equivalent ASCII data should be written to this register as soon as possible, and the Bit 7 should be written a 'one' as long as any key is held down, and changed to a 'zero' when the key is released.

The Apple // keyboard data flag is handled automatically by the logic in the Apple // Emulation Card gate-array. It will be set when data is written to the register, and cleared when the Apple // software accesses the proper soft-switch location(s) to clear the flag.

Reading back from this register is supported to facilitate testing.

6.1.9 THE READ DATA REPLACEMENT REGISTER - WRITE ONLY

Read/Write Addr: Base + xxx19 Size: 8-bits

This register allows the LC software to optionally replace the data that the Apple // would have read from a trapped address. For example, if the Apple // Emulation Card was trying to read from a hardware location on an I/O card, the LC could make it look to the Apple // Emulation Card like the hardware was present by supplying the appropriate data.

Reading back from this register is supported to facilitate testing.

Bits 0-7: 8 bits of data to optionally replace the data read during a trapped Apple //e read.

NOTE:

17. Writes to this register will be ignored unless the Apple // Emulation Card is currently trapped and in a read state. However, to avoid the possibility of a trap occuring at the same time the data is being written to the register, it should not normally be written to unless the Apple // Emulation Card is currently trapped.

Writes to this register automatically issue a "Go-Ahead" for the current trap and allow the 65C02 to continue running.

6.1.10 THE APPLE // ADDRESS LATCH / COUNTER REGISTER

Read-only Addr: Base + xxx1C Size: 16-bits

This register is actually a 16-bit counter that can be loaded by the LC software and used to address the Apple // Emulation Card memory when LC accesses it. Each time LC accesses the Apple //e memory the counter is automatically incremented.

Reading back from this location will return the current value in the Counter and is supported primarily to facilitate testing.

Bits 8-15: (Addr xx1C): Apple //e addresses 8-15 - The MS byte
Bits 0-7: (Addr xx1D): Apple //e addresses 0-7 - The LS byte.

6.1.11 THE APPLE // EMULATION CARD CONTROL REGISTER

Read-only Addr: Base + xxx20 Size: 16-bits

This register provides a mechanism so that the LC software can control various aspects of the Apple // Emulation Card hardware.

BIT	DESCRIPTION	BIT	DESCRIPTION
15	$\overline{\text{RESET}}$ to D.E.	7	Hires Pg1 trap enb.
14	$\overline{\text{NMI}}$ to D.E.	6	Hires pg2 trap enb.
13	$\overline{\text{IRQ}}$ to D.E.	5	TxtPg1 wrt trap enb.
12	HintEnb	4	TxtPg2 wrt trap enb.
11	$\overline{\text{SINGLESTEP}}$ mode	3	AuxMem Text/Lores write trap enb.
10	XTRA BIT output to pin	2	Aux Mem Hires write trap enb.
9	CA / PB1	1	JoyStick access trap enable
8	OA / PB0	0	$C8-Fxx trap enb.

NOTES:

18. The OA/PB0 and CA/PB1 bits simulate presses on the Open-Apple and Closed-Apple keys (also joystick PB0 and PB1) when set to '1's. These values are 'OR'd with actual pushbutton presses if a joystick is connected to the Apple // Emulation Card game port.
19. All bits in the control register are 'active high' so that '1's in the register activate the corresponding descriptions above.
20. The high byte (Bits 8-15) are accessed at loc. B+xxx20.
    The low byte (Bits 0-7) are accessed at loc. B+xxx21.
21. Reading back from this location is supported to facilitate testing and simply returns the last value written.

6.1.12 THE APPLE // CONTROL REGISTER

Read/Write Addr: $C02B Size: 8-bits

The Apple // Control Register is accessable from the 65C02 and not the Macintosh. It provides some additional functional controls not available from the normal soft-switches. '1's in the register bits cause the following actions:

BIT	DESCRIPTION
7	Output on SPARESSW pin from Gate-Array.
6	Disable External ROM port - access internal ROM space.
5	Enable Write to ROM areas if External ROM enabled.
4	Enable Alternate 64K Aux Bank
3	Enable Alternate DarkSide ROMbank
2	Enable Hi Speed 2 MHz mode - Per notes
1	Head Select output for 3.5" disks goes high.
0	$\overline{\text{SEL3.5}}$ Dsk output goes high.

NOTES:

22. When bit 2 is set, The 65C02 will be run at 2 MHz most of the time, rather than the normal 1 MHz. It will be run at 1 MHz when the Mac or the internal memory refresher are requesting memory cycles; and when the Slot 6 Disk Motor-On switch at $C0E8,9 is set and bit 0 - the 3.5" Disk select - is high.
23. The functions of Bits 3,4, and 5 are 'OR'ed with the corresponding function bits in the LC-Accessable Control registers.

6.2 THE MACINTOSH INTERFACE:

Apple // Emulation Card is designed to interface easily to the LC and other Macintosh computers. It will generate an internal 'Select' signal in response to the following patterns on its address inputs:

When FC(0-2) = 0-6

LC	FC3	A31	A27	A26	A25	A24	A23	A22	A21	A20
1	1	1	X	X	X	X	X	X	X	X
1	0	X	X	X	X	X	1	1	1	0
0	X	1	1	0	1	1	X	1	1	1

When the 'Select' condition is satisfied and the Mac asserts $\overline{AS}$, the Apple // Emulation Card will generate a $\overline{ROMSEL}$ and a $\overline{DSACK0}$ about 210ns later if the $\overline{CE}$ input is high, or allow access to the internal registers and eventually generate a $\overline{DSACK1}$ if the $\overline{CE}$ input is low and a valid register was accessed. If a valid register is not accessed $\overline{DSACK1}$ will not be generated. The Base address referred to in the previous register descriptions consists of the select condition and the $\overline{CE}$ input low when $\overline{AS}$ is asserted. The main purpose of the $\overline{CE}$ input is to provide support for an optional configuration ROM. If A19 is connected to the $\overline{CE}$ pin, accesses to the upper half of the card's 1 Meg address space will cause a $\overline{ROM}$ enable and a $\overline{DSACK1}$, and accesses to the lower half will enable the Apple // Emulation Card registers.

NOTE:

24. The time between $\overline{AS}$ input active and $\overline{DSACK0}$ or $\overline{DSACK1}$ outputs active will vary depending on the type of access and the point in the 65C02 timing cycle where the access is requested. Apple // Emulation Card does not use the Macintosh clock to develop its interface timing. Rather, the $\overline{AS}$ signal from the Macintosh is synchronized to the internal 14.31818MHz clock and this clock is used to generate the timing required. Accesses to internal registers and the 128K DRAM on the card also require additional time to come into sync with the 65C02 processor cycle.
    This method of operation avoids any bus or timing conflicts between the 65C02 and the 680XX in the Macintosh, but results in an indeterminate number of wait states for any given Apple // Emulation Card access cycle. In general, ROM cycles will have at least 200ns of wait state before $\overline{DSACK0}$ is generated, and Register or RAM access cycles will have no more than 1 µs of wait states.

6.3 REFERENCES: The following is a list of all the pertinent ASIC deliverables filed in Document Control:

1. Logic and pin-to-pin timing specifications for all LSI Logic macrocells and macrofunctions used in the Apple // Option Chip Gate-Array.
2. Functional and pin timing specifications for all compiled blocks such as ROM, RAM or PLA, in standard LSI Logic published format.
3. Two (2) magnetic tapes containing the schematic netlist file for those parts of the Apple // Option Chip Gate-Array that LSI Logic or Apple has sole ownership of and containing a list of those netfile names.
4. Logic diagram plot for those parts of the Apple // Option Chip Gate-Array which LSI Logic or Apple has sole ownership of and as supplied by Apple for those parts designed by Apple.
5. File of post-layout node and net capacitances and names for all circuit blocks that LSI Logic or Apple has sole ownership of.
6. Two (2) magnetic tapes of functional timing simulation inputs and outputs, including production test vectors, plus printed listing of file names.
7. Critical path timing analysis, including simulation results, if done by Apple and agreed by LSI Logic.
8. Two (2) database tapes for all mask layers created specifically for Apple, including cell interiors of those cells wherein LSI Logic of Apple has sole ownership, plus printed listing of file names.
9. Name of manufacturer and complete model designation of target test hardware and two (2) copies of the magnetic tape and printed listing of competed test program (production version, object code), plus printed listing of file names.
10. Two (2) copies (magnetic tape) of any existing high-level language test program, supporting documentation and file listings.
11. Load board and load board documentation, including schematics, description, mechanical drawings and target test hardware designation.
12. Bonding diagram.
13. Twenty-five (25) prototype units of the product in conformance with post-layout timing simulation and the design database.
14. All material owned solely by LSI Logic required to perfect ownership of the Maskworks and other Inventions assigned to Apple under this Agreement, including but not limited to (i) the supply of deposit materials required to register a Mask Work under the Semiconductor Chip Protection Act of 1984, Public Law 98-620, Chapter 9 of Title 17, United States Code, and/or, (ii) the supply of deposit materials required for registration of copyrights under Title 17, United States Code.